# Vortex86DX2

## 32-Bit X86 MicroProcessor



## Overview

The **Vortex86DX2** is a high performance and fully static 32-bit X86 processor with the compatibility of Windows based, Linux and most popular 32-bit RTOS. It also integrates 32KB write through 4-way L1 cache, 256KB write through/write back 4-way L2 cache, PCIE bus in at 2.5 GHz, DDR 3, ROM controller, ISA, I2C, SPI, IPC (Internal Peripheral Controllers with DMA and interrupt timer/counter included), Fast Ethernet,

FIFO UART, USB2.0 Host and IDE/SATA controller within a single 720-pin BGA package to form a system-on-a-chip (SOC). It provides an ideal solution for the embedded system and communications products (such as thin client, NAT router, home gateway, access point and tablet PC) to bring about desired performance.

## **Features**

#### ■ X86 Processor Core

- 6-stage pipeline

#### Floating point unit support

- Extends CPU instruction set to include Trigonometric, Logarithmic and Exponential
- Implements ANSI/IEEE standard 754-1985 for binary Floating-Point Architecture

#### **■** Embedded I / D Separated L1 Cache

16K I-Cache, 16K D-Cache

#### **■** Embedded L2 Cache

- 4-way 256KB L2 Cache
- Write through or write back policy

## ■ DDR3 Control Interface

- 32 bits data bus
- DDR3 clock support up to 400MHz
- DDR3 size support up to 2Gbytes

#### IDE Controller

PATA 100 ( Disk x 2 ) or SD Card x2

#### ■ SATA Controller

Supports 1 port serial ATA(1.5G)

#### ADC Interface x 8

#### ■ GPU Control Unit

- VGA controller
- 2D Graphics engine support
- UMA architecture

#### MAC Controller x 1

### ■ PCIE Control Interface x 2

- Up to 2 sets PCIE device
- 3.3V I/O

#### ■ ISA Bus Interface

- AT clock programmable
- 8/16 Bit ISA device with Zero-Wait-State
- Generate refresh signals to ISA interface during DRAM refresh cycle
- Support Max ISA Clock 33M
- HDA Controller
- DMA Controller
- Interrupt Controller
- **MTBF Counter**
- Counter / Timers
  - 2 sets of 8254 timer controller
  - Timer output is 5V tolerance I/O on 2<sup>nd</sup> Timer

## ■ Real Time Clock

 Less than 2uA (3.0V) power comsuption in Internal RTC Mode while chip is power-off.

### FIFO UART Port x 9 ( 9 sets COM Port )

- Compatible with 16C550 / 16C552
- Default internal pull-up
- Supports the programmable baud rate generator with the data rate from 50 to 6M bps
- The character options are programmable for 1 start bits; 1, 1.5 or 2 stop bits; even, odd or no parity; 5~8 data bits
- Support TXD\_En Signal on COM1/2
- Port 80h output data could be sent to COM1 by software programming

#### ■ Parallel Port x 1

Supports SPP/EPP/ECP mode

#### ■ General Programmable I/O

- Supports 88 programmable I / O pins
- Each GPIO pin can be individually configured to be an input/output pin
- GPIO\_P0~GPIO\_P4 can be program by 8051A
- GPIO\_P0~GPIO\_PA can be program by 8051B
- GPIO\_P0 and GPIO\_P1 with interrupt support (input/output)

#### ■ USB 2.0 Host Support

- Supports HS, FS and LS
- 4 port

#### ■ USB 1.1 Device Support

- 1 port
- Supports FS with 3 programmable endpoint

#### PS / 2 Keyboard and Mouse Interface Support

- Compatible with 8042 controller
- Speaker out
- Redundant System Support
- Embedded 2MB Flash
  - For BIOS storage

#### ■ I<sup>2</sup>C bus x 2

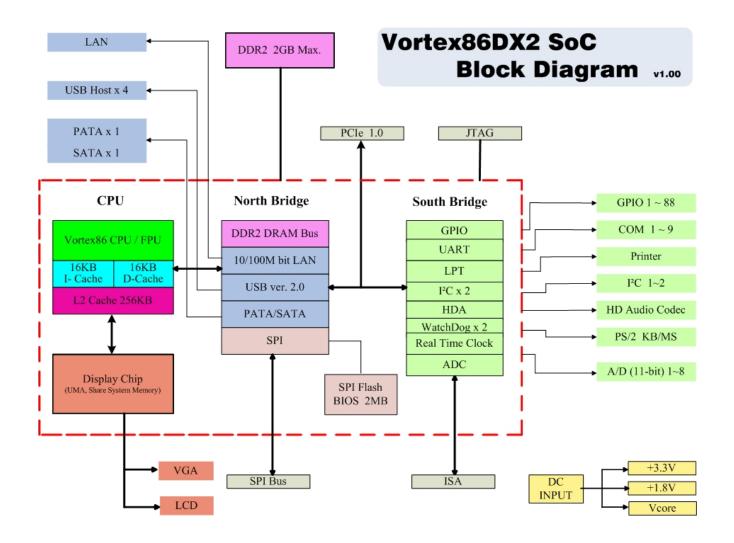
- Compliant w/t V2.1
- Some master code (general call, START and CBUS) not support.



- Motor Control Interface Support
  - 3 groups of controller, 4 controllers per group
  - Each controller can configure to PWM/Servo/Sensor Interface mode
  - Controller interconnect to the other with routing network in the same group
  - 8051 Internal Motion Control Support
- General Shift Interface Support
  - 3 channel
- JTAG Interface supported for S.W. debugging
- Input clock
  - 14.318 MHz
- Full Deplex SPI bus x 2

- 32.768 KHz
- Output clock
  - 24 MHz
  - 25 MHz
  - PCI clock
  - DDRII clock
- Operating Voltage Range
  - Core voltage: 1.0 V ± 5%
  - I / O voltage: 1.8V ± 5% , 3.3 V ± 10 %
- Operating temperature
  - TBD
- Package Type
  - 31x31mm, 720 Ball BGA

# **System Block Diagram**



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